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DISCLOSURE TEXT:

2p. It is possible to sputter chrome-copper-chrome circuitry onto both side of a ceramic wafer. As shown above, ceramic wafers 10 and 11 have circuitry 10A and 11A on the top side thereof and voltage or reference planes 10B and 11B on the lower side thereof. The substrates 10 and 11 and the reference planes 10B and 11B have holes 10C and 11C therein.

- Substrates 10 and 11 can be stacked on a base substrate 15 which has a matrix of pins 15C therein. The holes 10C and 11C correspond in location to the location of the pins 15C, whereby substrates 10 and 11 can be stacked on top of substrate 15, making a composite structure which has two layers of circuity 10A and 11A, each of which has an associated ground plane 10B and 11B located relatively close thereto.

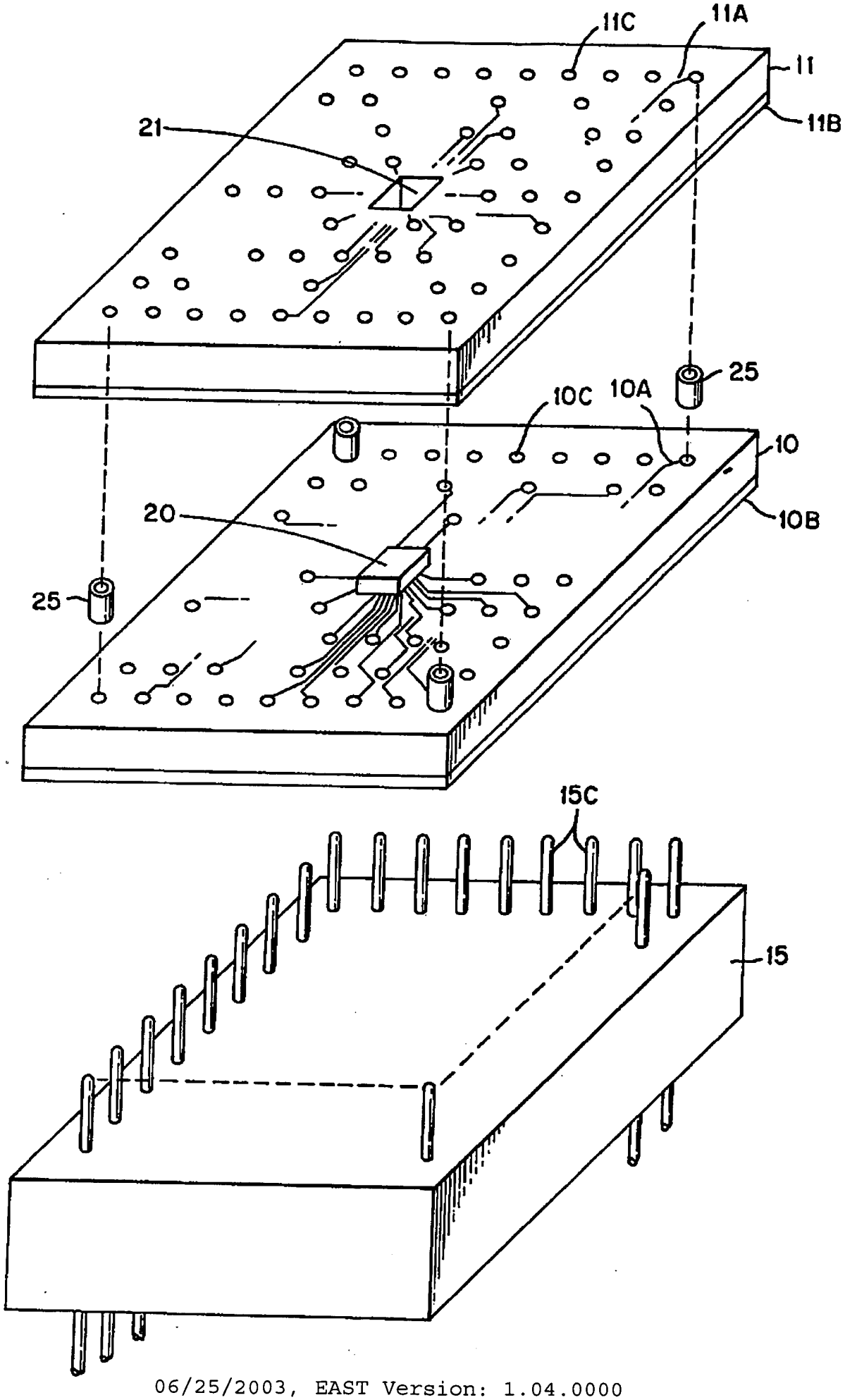
- An integrated circuit 20 is mounted on substrate 10, and an opening 21 is provided in substrate 11 to accommodate integrated circuit 20.

- Separation of the substrates may be accomplished by a selected pin upset for a standoff feature or by the use of glass or ceramic beads 25.

- Rather than having planes 10B and 11B merely serve as reference or voltage ground planes, circuitry can also be etched in these layers. Furthermore, substrate 11 can be positioned close enough to substrate 10 that circuitry in layer 11B can be interconnected with circuitry in layer 10A by solder ball technology.

- The sputtered metal process also coats the hole walls, producing electrical conductivity between both sides of the ceramic wafer. Etched isolation rings in the metal around the holes 10C and 11C ;may selectively prevent electrical contact with pins 15C. Other holes not on the 15C pin matrix may be used for inter-surface

electrical connection.


11C
11A
11
11B
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10C
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